

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Rule 53(b) Divisional Application of:

Taiji EMA et al.

Divisional of S.N. 09/637,256 filed August 14, 2000

Group Art Unit: To Be Assigned

Filed: Herewith

Examiner: To Be Assigned

For: SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR FABRICATING THE SAME

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 CFR 1.97(b)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

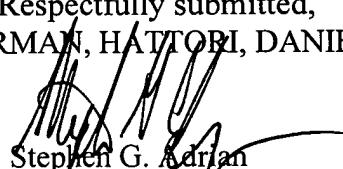
Date: March 11, 2004

Sir:

This Information Disclosure Statement is being filed in order to comply with Applicant's duty of disclosure under 37 CFR 1.56. The documents listed on the Form PTO-1449 were made of record in parent application Serial No. 09/637,256.

The Commissioner is authorized to charge our Deposit Account No. 50-2866 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,  
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<b>INFORMATION DISCLOSURE CITATION</b>	Atty. Docket No. <b>960045E</b>	Serial No. <b>To be assigned</b>
	Applicant(s): <b>Taiji EMA et al.</b>	
	Filing Date: <b>Herewith</b>	Group Art Unit: <b>To be assigned</b>

**PTO-1449**

**U.S. PATENT DOCUMENTS**

Examiner	Document No.	Name	Date	Class	Subclass	Filing Date
Initial	(If appropriate)					
AB	5,502,336	Park et al.	03/96			
AC	5,479,054	Tottori	12/95			
AD	5,338,700	Dennison et al.	08/94			
AE	4,974,040	Taguchi et al.	11/90			
AF	5,150,278	Gonzallez et al.	09/92			
AG	5,196,910	Moriuchi et al.	03/93			
AH	5,605,857	Jost et al.	02/97			
AI	5,324,681	Lowrey et al.	06/94			
AJ	5,292,677	Dennison	03/94			
AK	5,281,549	Fazan et al.	01/94			
AL						
AM						

**FOREIGN PATENT DOCUMENTS**

Document No.	Date	Country	Translation (Yes or No)
AN 61-176148	08/07/96	Japan	
AO 3-167874	07/19/91	Japan	
AP 5-218332	08/27/93	Japan	
AQ			

## OTHER DOCUMENTS

_____	AR	B.LUTHER et al.; "Planar Copper-Polyimide Back End of the Line"; Proceedings of 10 <sup>th</sup> International VMIC; pages 15-21; June 1993.
_____	AS	B.M. SOMERO et al.; "A Modular in-situ Integration Scheme for Deep Submicron", Proceedings of 10 <sup>th</sup> International VMIC; pages 28-34; June 1993.
_____	AT	M.F. CHISHOLM et al.; "A High Performance 0.5 um Five-Level Metal Process with Extendibility of Sub-Half Micron"; pages 22-28; June 1994.
_____	AU	M. RUTTEN et al.; "Pattern Density Effects in Tungsten CMP", Proceedings of 12 <sup>th</sup> International VMIC; pages 491-497; June 1995.
_____	AV	I. NAIKI et al.; "Center Wordline Cell: A New Symmetric Layout Cell for 64Mb SRAM"; Technical Digest of IEDM; pages 817-820; December 1993.
_____	A W	T. KAGA et al.; "A 0.29-um <sup>2</sup> MIM-Crown Cell and Process Technologies for 1-Gigabit DRAMs"; Technical Digest of IEDM; pages 927-929; December 1994.
_____	AX	H.K. KANG et al.; "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs"; Technical Digest of IEDM; pages 635-638; December 1994.
_____	A Y	Y. OHJI et al.; "Ta <sub>2</sub> O <sub>5</sub> Capacitors Dielectric Material for Giga-bit DRAMs"; Technical Digest of IEDM; pages 111-114; December 1995.
_____	AZ	Y. NISHIOKA et al.; "Giga-bit Scale DRAM Cell with New Simple Ru/(Ba,Sr)TiO <sub>3</sub> /Ru Stacked Capacitors Using X-ray Lithography"; Technical Digest of IEDM; pages 903-906; December 1995.
_____	BA	K.P. LEE et al.; "A Preocess Technology for 1 Giga-bit DRAM"; Technical Digest of IEDM; pages 907-910; December 1995.
_____	BB	J.K. PARK et al.; "Isolation Merged Bit Line Cell(IMBC) for 1Gb DRAM and Beyond". Technical Digest of IEDM; pages 911-914; December 1995.
_____	BC	
_____	BD	

Examiner

Date Considered